1. Introduction

This document provides quickstart information and main features about RVS Module v. 1.0.

The RVS Module v. 1.0 is a low-cost vision system for acquisition and real-time processing of pictures.

The module main devices are: a ST-VS6724 Camera (2 Mpx), a ST-STR912FA Microcontroller (ARM966 @ 96MHz) and 16MB of external RAM (PSRAM BURST).

The embedded microcontroller allows the syncronization of multiple modules for multi-camera vision (or simply stereo vision) and the execution of various vision algorithms such as multiple blob search, vision SLAM and robot navigation.
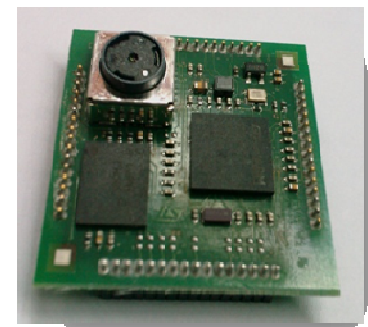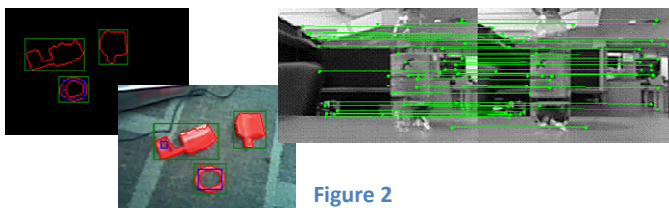
Figure 1

Figure 2

Multiple Blob Search and Stereo Vision

Figure 3

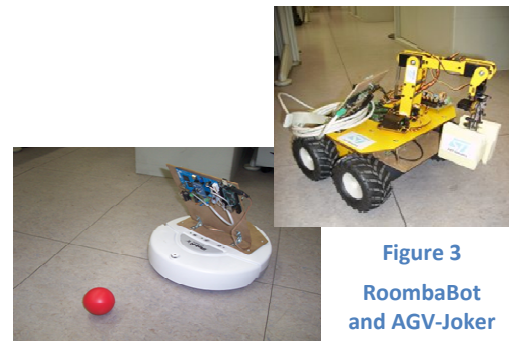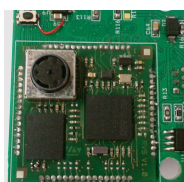**RoombaBot and AGV-Joker demo**

Two different configurations are available, as shown below:

(Figure 4.a)

Socket Version: 34 x 34 mm, with a 64 pins connector (16 per edge), suitable for application prototyping.

(Figure 4.b)

System-on-Module (SoM) Version: 30 x 30 mm, with 64 contact pins, directly solderable as a surface-mount device (SMD), suitable for application production.

2. Main components overview

ST-STR912FAZ44 Microcontroller:

Figure 5

The ST-STR912FAZ44 embedded controller is ideal for a wide variety of applications such as point-of-sale terminals, industrial automation, security and surveillance, vending machines, communication gateways, serial protocol conversion, and medical equipment.

The microcontroller main components are: a 32 bit ARM966E-S RISC processor core running at 96MHz, a large 32bit SRAM (96KB) and a high-speed 544KB Flash memory.

The ARM966E-S core can perform single-cycle DSP instructions, good for speech recognition, audio and embedded vision algorithms.

Features

- 16/32-bit 96 MHz ARM9E based MCU
  - ARM966E-S RISC core: Harvard architecture, 5-stage pipeline, Tightly-Coupled Memories (SRAM and Flash)
  - STR91xFA implementation of core adds high-speed burst Flash memory interface, instruction pre-fetch queue, branch cache
  - Up to 96 MIPS directly from Flash memory
  - Single-cycle DSP instructions supported
  - Binary compatible with ARM7 code
- Dual burst Flash memories, 32-bits wide
  - 512 KB Main Flash and 32 KB Secondary Flash
  - Sequential Burst operation up to 96 MHz
  - 100 K min erase cycles, 20 yr min retention
- SRAM, 32-bits wide at 96 K bytes
- 9 programmable DMA channels
- Clock, reset, and supply management
  - Internal oscillator operating with external 4-25 MHz crystal
  - Internal PLL up to 96 MHz
  - Real-time clock provides calendar functions, tamper, and wake-up functions
  - Reset Supervisor monitors supply voltage, watchdog, wake-up unit, external reset
  - Brown-out monitor
  - Run, Idle, and Sleep Mode as low as 50 uA
- Vectored interrupt controller (VIC)
  - 32 IRQ vectors, 30 interrupt pins

- – Branch cache minimizes interrupt latency
- 8-channel, 10-bit A/D converter (ADC)
  - – 0 to 3.6 V range, 0.7 usec conversion
- 10 Communication interfaces
  - – 10/100 Ethernet MAC with DMA and MII
  - – USB Full-speed (12 Mbps) slave device
  - – CAN interface (2.0B Active)
  - – 3 16550-style UARTs with IrDA protocol
  - – 2 Fast I2C™, 400 kHz
  - – 2 channels for SPI™, SSI™, or Microwire™
- External Memory Interface (EMI)
  - – 8- or 16-bit data, up to 24-bit addressing
  - – Additional burst synchronous modes
- I/O pins (muxed with interfaces)
- 16-bit standard timers (TIM)
  - – 4 timers each with 2 input capture, 2 output compare, PWM and pulse count modes
- 3-Phase induction motor controller (IMC)
- JTAG interface with boundary scan
- Embedded trace module (ARM ETM9)

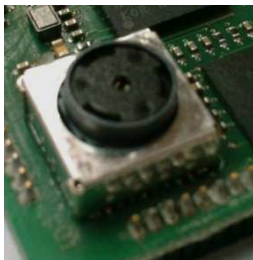## ST-VS6724 Camera Module:

Figure 6

Figure 7

The VS6724 is a UXGA resolution CMOS imaging device designed for low power systems, particularly mobile phone and PDA applications. Manufactured using ST 0.18 μm CMOS Imaging process, it integrates a high-sensitivity pixel array, digital image processor and camera control functions.

The device contains an embedded video processor and delivers fully color processed images at up to 30 fps UXGA JPEG, or up to 30 fps SVGA YCbCr 4:2:2. The video data is output over an 8-bit parallel bus in JPEG (4:2:2 or 4:2:0), RGB, YCbCr or Bayer formats and the device is controlled via an I²C interface.

The VS6724 support 1.8 V or 2.8 V interface and requires a 2.4 to 3.0 V analog power supply. The integrated PLL allows for low frequency system clock, and flexibility for successful EMC integration. The VS6724 camera module uses ST's second generation "SmOP2" packaging technology: the sensor, lens and passives are assembled, tested and focused in a fully automated process, allowing high volume and low cost production.
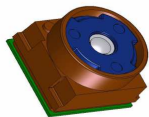
The VS6724 also includes a wide range of image enhancement functions, designed to ensure high image quality, these include: automatic exposure control, automatic white balance, lens shading compensation, defect correction algorithms, interpolation (Bayer to RGB conversion), color space conversion, sharpening, gamma correction, flicker cancellation, NoRA noise reduction algorithm, intelligent image scaling, special effects.

Features

- 1600H x 1200V active pixels
- Class leading 30 fps UXGA progressive scan
- μm pixel size, 1/3.8 inch optical format
- Quad-element plastic lens, F# 3.2, 52° horizontal field of view (HFOV)
- 8.0 x 8.0 x 5.55 mm ultra low profile fixed focus camera module with embedded passives
- RGB Bayer color filter array
- Integrated 10-bit ADC
- Integrated digital image processing functions
- Embedded hardware JPEG compression (4:2:0 or 4:2:2) delivering 30 fps streaming performance
- Embedded camera controller for automatic exposure control, automatic white balance control, black level compensation, 50/60 Hz flicker cancelling, flashgun support
- Fully programmable frame rate and output derating functions
- Low power 30 fps up to SVGA for video capture
- ITU-R BT.656-4 YUV (YCbCr) 4:2:2 with embedded syncs, YUV (YCbCr) 4:0:0, RGB 565, RGB 444, JPEG, Bayer 10-bit or Bayer 8-bit output formats
- 8-bit parallel video interface, horizontal and vertical syncs, 80 MHz (max) clock
- Two-wire serial control interface (I^2C)
- On-chip PLL, 6.5 to 27 MHz clock input
- Analog power supply, from 2.4 V to 3.0 V
- Separate I/O power supply, 1.8 V or 2.8 V levels
- Integrated power management with power switch, automatic power-on reset and powersafe pins
- Low power consumption, ultra low standby current
- 24-pin 8.0 mm x 8.0 mm x 5.55 mm shielded socket

16 MB external burst PSRAM 100MHz (mod. MT45W8MW16BGX):

This PSRAM is a high-speed, CMOS pseudo-static random access memory developed by Micron® CellularRAM™ for low-power, portable applications. On ST-RVS Module v . 0.1 it allow handling of high quantity of data concerning images processing and storage.

The MT45W8MW16BGX device has a 128Mb DRAM core, organized as 8 Meg x 16 bits. These devices include an industry standard burst mode Flash interface that highly increases read/write bandwidth.

To operate seamlessly on a burst Flash bus, the PSRAM incorporate a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance. The bus configuration register (BCR) defines how the device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. Standby current consumption during self refresh is minimized.

The CellularRAM bus interface supports both asynchronous and burst mode transfers.

Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

Features:

- Single device supports asynchronous, page, and burst operations
- VCC, VCCQ voltages
    - 1.70–1.95V VCC
    - 1.7–3.6V1 VCCQ
- Random access time: 70ns
- Burst mode READ and WRITE access
    - 4, 8, 16, or 32 words, or continuous burst
    - Burst wrap or sequential
    - MAX clock rate: 133 MHz (tCLK = 7.5ns)
    - Burst initial latency: 35ns (5 clocks) at 133 MHz
    - tACLK: 5.5ns at 133 MHz
- Page mode READ access
    - Sixteen-word page size
    - Interpage READ access: 70ns
    - Intrapage READ access: 20ns
- Low power consumption
    - Asynchronous READ: <25mA
    - Intrapage READ: <15mA
    - Initial access, burst READ: (37.5ns [5 clocks] at 133 MHz) <45mA
    - Continuous burst READ: <40mA
    - Standby: <50µA (TYP at 25°C)
    - Deep power-down: <3µA (TYP)
- Low-power features
    - On-chip temperature-compensated refresh (TCR)
    - Partial-array refresh (PAR)
    - Deep power-down (DPD) mode
- Configuration
    - 8 Meg x 16 MT45W8MW16B
    - VCC core voltage: 1.70–1.95V
    - VCCQ I/O voltage: 1.7–3.6V1
- Timing
    - 70ns access –70
    - 85ns access –85
- Frequency
    - 66 MHz 6
    - 80 MHz 8

- 104 MHz 1
- 133 MHz 13
- Standby power at 85°C
  - Standard: 200µA (MAX) None
  - Low power: 160µA (MAX) L
- Operating temperature range
  - Wireless (−30°C to +85°C) WT

3. RVS Module v.1.0 pin connections:

Figure 8

P/N	Pin Name	Function	Description
1	3V3_CAM	Camera power supply (3.3V)	Camera typical power supply is 2.8V. Conversion from 3.3V to 2.8V is accomplished by a LDO voltage regulator embedded on the module.
2	MII_COL	MII (Media Independent Interface)	The Media Independent Interface (MII) is a standard interface used to connect a Fast Ethernet (for data transfer at 10 Mb/s and 100 Mb/s) MAC-block to a PHY. Being media independent means that any of several different types of PHY devices can be used without redesigning or replacing the MAC hardware.
3	MII_CRS		
4	MII_TXD2		
5	MII_TXD3		
6	MII_TXD0		
7	MII_TXD1		
8	GROUND	Ground	
9	MII_TXCLK	MII (Media Independent Interface)	
10	MII_TXEN		
11	MII_RXER		
12	MII_CLK		
13	MII_RXDV		
14	MII_RXCLK		
15	MII_RXD1		
16	GROUND	Ground	
17	1V8_RAM	RAM power supply (1.8V)	Core voltage for MT45W8MW16BGX PSRAM
18	MII_RXD0	MII (Media Independent Interface)	
19	MII_RXD3		
20	MII_RXD2		
21	MII_MDIO		
22	MII_MDC		
23	TAMPER	Tamper detect input pin	Tamper input pin is used to detect and record the time of a tamper event on the end product such as malicious opening of an enclosure, unwanted opening of a panel, etc. Once a tamper event occurs, the RTC time (millisecond resolution) and the date are recorded in the RTC unit. Simultaneously, the SRAM standby voltage source will be cut off to invalidate all SRAM contents.

24	GROUND	Ground	
25	JTRST		
26	JTDI		An IEEE-1149.1 JTAG interface on the STR91xFA provides In-System-Programming (ISP) of all memory, boundary scan testing of pins, and the capability to debug the CPU.
27	JTMS	JTAG peripheral	
28	JTCK		
29	JRTCK		
30	JTDO		
31	RESET_IN	Reset	General reset of device
32	GROUND	Ground	
33	3V3_RAM	RAM power supply (3.3V)	I/O voltage for MT45W8MW16BGX PSRAM
34	PO_I2C1_SCL		An I2C Bus Interface serves as an interface between the microcontroller and the serial I2C bus. It provides both multimaster and slave functions, and controls all I2C bus-specific sequencing, protocol, arbitration and timing.
35	PO_I2C1_SDA	I^{2}C device	
36	PO_SSP0_SCLK		The SSP is a master or slave interface for synchronous serial communication with peripheral devices that have either Motorola SPI, National Microwire or Texas Instruments SSI synchronous serial interfaces.
37	PO_SSP0_MOSI	SSP (Syncronous Serial Peripheral) n°0	
38	PO_SSP0_MISO		
39	PO_SSP0_NSS		
40	GROUND	Ground	
41	PO_DMA_REQ1	DMA Trigger	Allow DMA trigging with external clock.
42	PO_U1RX_CANTX		Possibility to choose UART or CAN peripheral connection. The UART interface provides serial communication between the STR91xF and other
43	PO_U1TX_CANRX	UART or CAN peripheral	microcontrollers, microprocessors or external peripherals. It supports full-duplex asynchronous communication. The CAN peripheral consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The bit rate can be programmed to values up to 1MBit/s.
44	PO_SSP1_SCLK		The SSP is a master or slave interface for synchronous serial communication with peripheral devices that have either Motorola SPI, National Microwire or Texas Instruments SSI synchronous serial interfaces.
45	PO_SSP1_MISO	SSP (Syncronous Serial Peripheral) n°1	
46	PO_SSP1_MOSI		
47	PO_SSP1_NSS		
48	GROUND	Ground	
49	3V3_uC	Microcontroller power supply (3.3V)	Operating voltage for STR912 I/O ring
50	V_BATT		
51	V_R_A		
52	1V8_uC	Microcontroller power supply (1.8V)	Operating voltage for STR912 core and internal RAM
53	PO_ADC0		The Analog-to-Digital Converter (ADC) comprises an input multiplexed channel selector feeding a successive approximation converter. The conversion resolution is 10 bits.
54	PO_ADC1	ADC (Analog-to-Digital Converter)	
55	PO_SYNC_OUT	Syncronization Output pin	In multiple camera synchronization applications this pin is used to clock all the cameras.
56	GROUND	Ground	
57	PO_ADC3	ADC (Analog-to-Digital Converter)	
58	PO_SYNC_IN	Syncronization Input pin	In multiple camera synchronization applications this pin is used to read the external clock.
59	USB_DN		The USB slave interface consists of both the USB Serial Interface Engine (SIE) and the USB Transceiver (Physical interface).
60	USB_DP	USB peripheral (USB2 full-speed)	
61	PO_USB_CTL		
62	PO_U0TX_CANRX		
63	PO_U0RX_CANTX	UART or CAN peripheral	
64	GROUND	Ground	

4. RVS Main Board:

The RVS Main Board is an application board specifically designed to evaluate the RVS Module.

The main features of this board are:

- JTAG
- High Luminosity LED
- Ethernet 10/100 port
- USB2 full-speed
- CAN2.0B
- 2 x RS232
- Fast IR port
- MicroSD card socket
- I^2C
- SPI
- GPIOs
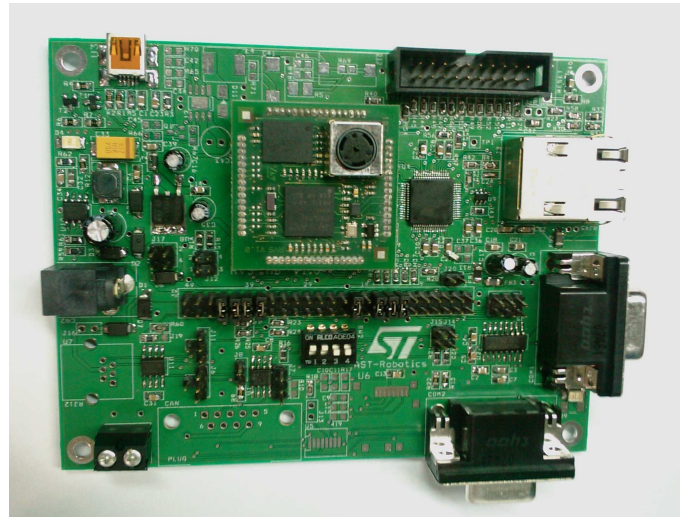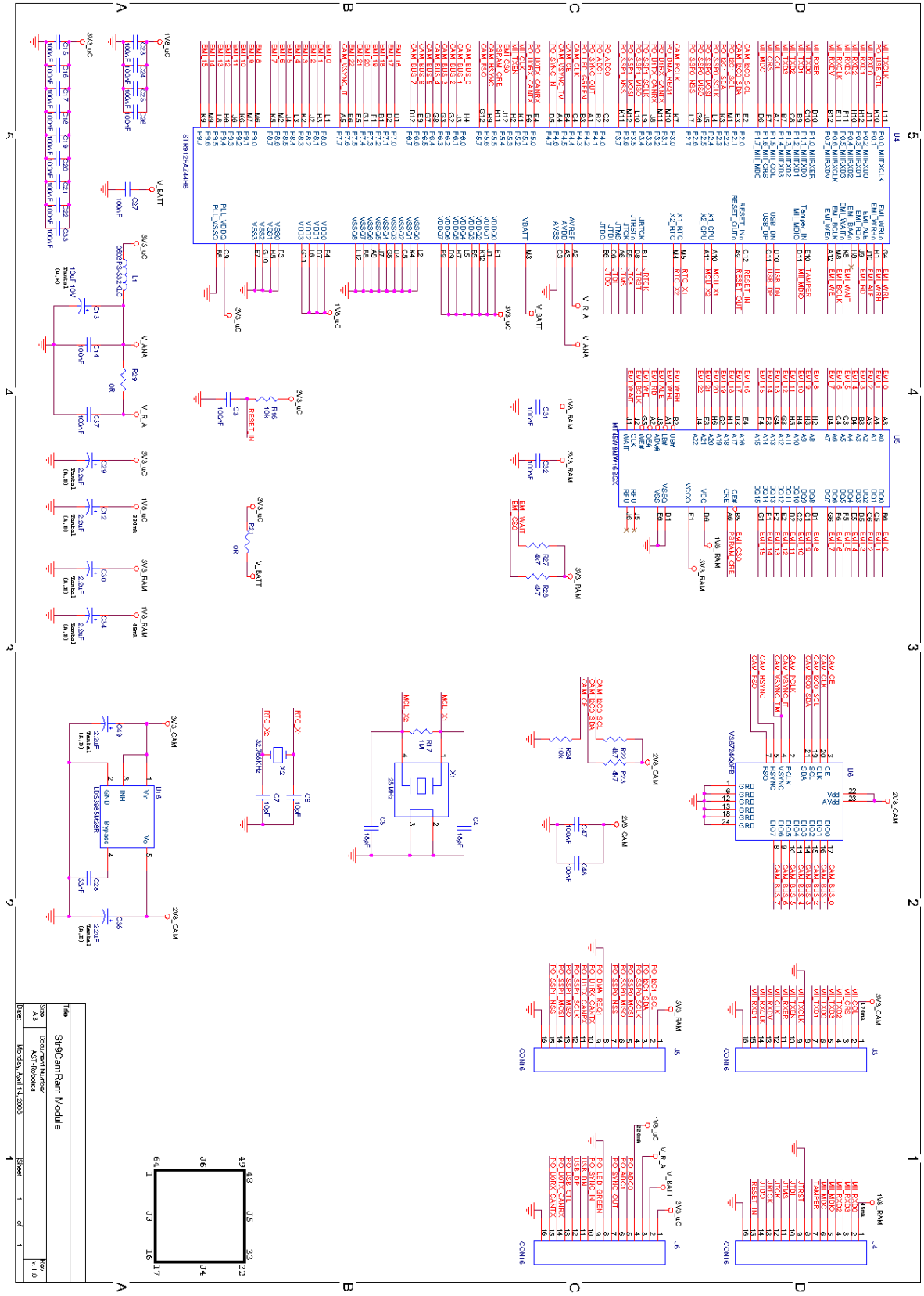- Lego NXT interface port (RS485/I^2C)
- Multiple-camera synchronization port

Figure 9

The RVS Module v. 1.0 - Socket Version is installed in the center of board (as shown in the above picture).

Board dimensions: 120 x 90 mm.

5. RSV Module v. 1.0 schematic:

Figure 10

6. Bill of materials

Chips

Part	Package	Detail description	Order code (reference)
U4	LFBGA144	STR912FAZ44H6	STM
U5	VFBGA54	PSRAM 70ns 104MHz 128Mbit	MT45W8MW16BCGB-701WT Micron
U6 part 1/3	SmOP2	VS6724Q0FB	STM
U6 part 2/3		SMK Socket per VS6724	CLE9124-1501FSZ SMK
U6 part 3/3		SMK Lid per VS6724	CLE9124-1401F SMK
U16	SOT23-5	LDS3985M28R	STM

Capacitors

Part	Package	Detail description	Order code (reference)
C6, C7	0402	Chip capacitor 10pF 50V COG	GRM1555C1H180JZ01D Murata
C4, C5	0402	Chip capacitor 18pF 50V COG	GRM1555C1H180JZ01D Murata
C28	0402	Chip capacitor 33nF 10V X7R	GRM155R71A333KA01 Murata
C3, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C31, C32, C33, C37, C47, C48	0402	Chip capacitor 100nF 10V X5R	GRM1555R61A104KA01D Murata AVX
C12, C29, C30, C34, C38, C49	0402	Tantalum capacitor 2.2uF / 6.3V	TACK225M006RTA AVX
C13	0603	Tantalum capacitor 10uF / 6.3V	TACL106M006RTA AVX

Resistors

Part	Package	Detail description	Order code (reference)
R21, R29, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55	0402	0 ohm	
R22, R23, R27, R28	0402	4.7K 5%	
R16, R24	0402	10K 1%	
R17	0402	1M 1%	

Inductor

Part	Package	Detail description	Order code (reference)
L1	0603	Chip inductor 3.3uH	0603PS-332KLC Colicraft

Xtal

Part	Package	Detail description	Order code (reference)
X1	2.5 x 2.0mm	Xtal 25MHz ±10ppm tolerance, ±25ppm stability, cload 10pF	NDK
X2	3.2 x 1.5mm	Crystal 32.768KHz	CC7V-T1A-0.5 Micro Crystal

Connectors

Part	Package	Detail description	Order code (reference)
J3, J4, J5, J6	20.3 x 2.5mm	16 pin strip connector female pitch 1.27 mm	W53481116SA Winslow AdaptICs

7. Revision history

Document revision history

Date	Revision	Changes
24-Nov-2008	1.0	Initial release
27-Nov-2008	2.1	Schematic update, adding of chap. 6

8. Appendix